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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,074	03/30/2004	Clinton F. Walker	42P18956	5486

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EXAMINER	
SPITTLE, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,074	WALKER ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 5 and 8 – 14 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui (U.S. 7,155,627) in view of Yoo et al. (U.S. 6,834,014) and Janzen (U.S. 7,142,461).

Regarding claim 1, Matsui teaches a dynamic random access memory device comprising:

An address bus interface (112);

A data bus interface (111);

Matsui teaches a termination circuit (Fig. 3, see termination resistor at end of daisy chain; Fig. 19), but fails to teach it being enabled or disabled, as well as a termination control signal input to control it.

Yoo et al. teach a termination circuit that can be enabled or disabled (Fig. 4, 420, 440; col. 5, line 57 – col. 6, line 13); and

a termination control signal input (Figure 2; where the input is interpreted as the input to the switches SW3, SW4, SW5, SW6 connected to items CON1, CON2) wherein the termination control signal input is operable to enable the termination circuit when the termination control signal input is tied to a first voltage level, and wherein the termination control signal input is operable to disable the termination circuit when the termination control signal input is tied to a second voltage level (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Yoo et al. provides the suggestion that the termination control circuitry could be applied to an address bus and a data bus (col. 4, lines 27 – 29).

Yoo et al., however, does not teach using the termination circuitry in a system of daisy chained memory devices as in Matsui.

Janzen teaches using active termination circuitry in a daisy-chained memory system (Figs. 2, 5) for the purpose of providing flexible termination for preventing signal reflections while not requiring a larger number of pin connections in an electronic system (col. 1, lines 48 – 51; col 15, lines 23 – 27).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the termination means of Yoo et al. into the memory system of Matsui for the purpose of terminating a memory bus flexibly when the configuration changes (col. 1, line 47 – col. 2, line 11). This would have been obvious in order to increase the reliability and performance of the memory bus.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the termination means of Janzen into the memory system of Matsui and Yoo et al. for the purpose of providing active termination control that is flexible, prevents signal reflections, and does not require a large number of pin connections in order to do so. This would have been obvious to increase the reliability and performance of the memory bus, as well as reduce the cost of doing so.

Regarding claim 2, Yoo et al. teach the additional limitation where the address bus termination circuit to be enabled if an asserted address bus termination control signal (Figure 2, items CON1, CON2) is received at the address bus termination control signal input (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 3, Yoo et al. teach the additional limitation where the address bus termination circuit to be disabled if the address bus termination circuit control signal

(Figure 2, items CON1, CON2) is not asserted (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 4, Yoo et al. teach the additional limitation wherein the address bus termination control signal (Figure 2, items CON1, CON2) is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

* * *

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo et al. (U.S. 6,834,014) in view of Janzen et al. (U.S. 6,538,951).

Regarding claim 5, Yoo et al. fail to teach wherein the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level.

Janzen et al. teach that it is well known in the art to reverse logic states (column 2, lines 25 – 33) since one permutation may permit a simpler, yet functionally equivalent design.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the memory device of Yoo et al. to reverse logic states as taught by Janzen et al., and designate the control signal as being asserted when at a logically low level instead of a logic high level. This would have been obvious in order to permit a simpler, yet functionally equivalent design.

* * *

Claims 8 – 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui (U.S. 7,155,627) in view of Yoo et al. (U.S. 6,834,014) and Janzen (U.S. 7,142,461).

Regarding claim 8, Matsui teaches a plurality of dynamic random access memory devices coupled to an address bus in a daisy chain configuration, each of the plurality of dynamic random access memory devices including:

An address bus interface (112);

A data bus interface (111);

Matsui teaches a termination circuit (Fig. 3, see termination resistor at end of daisy chain; Fig. 19), but fails to teach it being enabled or disabled, as well as a termination control signal input to control it.

Yoo et al. teach a termination circuit that can be enabled or disabled (Fig. 4, 420, 440; col. 5, line 57 – col. 6, line 13); and

a termination control signal input (Figure 2; where the input is interpreted as the input to the switches SW3, SW4, SW5, SW6 connected to items CON1, CON2) wherein the termination control signal input is operable to enable the termination circuit when the termination control signal input is tied to a first voltage level, and wherein the termination control signal input is operable to disable the termination circuit when the termination control signal input is tied to a second voltage level (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Yoo et al. provides the suggestion that the termination control circuitry could be applied to an address bus and a data bus (col. 4, lines 27 – 29).

Yoo et al., however, does not teach using the termination circuitry in a system of daisy chained memory devices as in Matsui.

Janzen teaches using active termination circuitry in a daisy-chained memory system (Figs. 2, 5) for the purpose of providing flexible termination for preventing signal reflections while not requiring a larger number of pin connections in an electronic system (col. 1, lines 48 – 51; col 15, lines 23 – 27).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the termination means of Yoo et al. into the memory system of Matsui for the purpose of terminating a memory bus flexibly when

the configuration changes (col. 1, line 47 – col. 2, line 11). This would have been obvious in order to increase the reliability and performance of the memory bus.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the termination means of Janzen into the memory system of Matsui and Yoo et al. for the purpose of providing active termination control that is flexible, prevents signal reflections, and does not require a large number of pin connections in order to do so. This would have been obvious to increase the reliability and performance of the memory bus, as well as reduce the cost of doing so.

Regarding claim 9, Yoo et al. teach the additional limitation where the address bus termination circuit to be enabled if an asserted address bus termination control signal (Figure 2, items CON1, CON2) is received at the address bus termination control signal input (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 10, Yoo et al. teach the additional limitation where the address bus termination circuit to be disabled if the address bus termination circuit control signal (Figure 2, items CON1, CON2) is not asserted (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination

resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 11, Yoo et al. teach the additional limitation wherein the address bus termination control signal (Figure 2, items CON1, CON2) is asserted when at a logically high voltage level and is not asserted when at a logically low voltage level (column 7, lines 40 – 44 describe where the control signal CON being at a first voltage level (low level) and the termination resistor being OFF; column 8, lines 5 – 10 describe where the control signal CON is at a second voltage level (high level) and the termination resistor is turned ON).

Regarding claim 12, Yoo et al. teach the additional limitation wherein all but the last memory device has its address bus termination control signal input tied to a positive voltage and the last memory device in the daisy chain configuration has its address bus termination control signal tied to ground (where a positive voltage may be interpreted as a logic high level, and a ground may be interpreted as a logic low level (Fig. 7, see row labeled "1-RANK/1-RANK", and more particularly, the sub-row named "OPERATION TO: MODULE 1" which shows how the first module is turned off while the last module is turned on. The signal levels of the control signals (CON1, CON2) are further described in col. 7, lines 40 – 44, and col. 8, lines 5 – 9). Yoo et al. fail to teach the daisy chain connection, though Janzen and Matsui do teach this configuration. Examiner takes

official notice that it is well known in this art to apply termination at the end of a daisy chain of memory devices. This is evidenced in Matsui (Fig. 3).

Regarding claim 14, Yoo et al. teach the additional limitation wherein all but the last memory device has its address bus termination control signal input tied to a positive voltage and the last memory device in the daisy chain configuration has its address bus termination control signal tied to ground (where a positive voltage may be interpreted as a logic high level, and a ground may be interpreted as a logic low level (Fig. 7, see row labeled "1-RANK/1-RANK", and more particularly, the sub-row named "OPERATION TO: MODULE 2" which shows how the first module is turned on while the last module is turned off. The signal levels of the control signals (CON1, CON2) are further described in col. 7, lines 40 – 44, and col. 8, lines 5 – 9). Yoo et al. fail to teach the daisy chain connection, though Janzen and Matsui do teach this configuration. Examiner takes official notice that it is well known in this art to apply termination at the end of a daisy chain of memory devices. This is evidenced in Matsui (Fig. 3).

* * *

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoo et al. (U.S. 6,834,014) in view of Janzen et al. (U.S. 6,538,951).

Regarding claim 13, Yoo et al. fail to teach wherein for each of the plurality of memory devices the address bus termination control signal is asserted when at a logically low voltage level and is not asserted when at a logically high voltage level.

Janzen et al. teach that it is well known in the art to reverse logic states (column 2, lines 25 – 33) since one permutation may permit a simpler, yet functionally equivalent design.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the memory device of Lewis et al. to reverse logic states as taught by Janzen et al., and designate the control signal as being asserted when at a logically low level instead of a logic high level. This would have been obvious in order to permit a simpler, yet functionally equivalent design.

Response to Arguments

Applicant's arguments filed 1/3/2007, with respect to the rejection(s) of claim(s) 1 – 14 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Matsui (U.S. 7,155,627) and Janzen (U.S. 7,142,461).

Examiner notes that Matsui teaches separate data bus (111) and address bus interfaces (112) and Yoo et al., cited from the previous office action, provides suggestion to use termination circuitry with both (col. 4, lines 27 – 28).

Regarding Applicant's amendment to claims 1 and 8 that now recite, "a dynamic random access device...", Examiner notes that Yoo et al., Matsui, and Janzen all pertain to dynamic random access memory systems.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MDS

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